REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. In the Specification, the title has been amended. In the Claims, claims 1, 8, 10-11, 14, 16, and 29 were previously amended; and claim 9 was previously cancelled. Existing claims 1-8 and 10-30 remain in the application. Please note that the prosecuting attorney for this application has been changed.

ARGUMENT

Title

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title has been amended. Applicants submit that the currently amended title is descriptive and clearly indicative of the invention to which the claims are directed.

Claim Rejections – 35 U.S.C. § 102

Claims 23-30 are rejected under 35 U.S.C. § 102(b) as being anticipated by Levy et al. (U.S. Patent No. 6,092,175) (hereinafter Levy).

First, the Examiner asserted that Fig. 15 of Levy discloses the limitation of initializing a register allocation table (RAT) to map a first group of logical registers to a second group of physical registers. Applicants respectfully disagree. As Fig. 15 of Levy clearly shows, Fig. 15 a figure illustrating a mapping relationship from references to architectural registers in instructions to renaming registers. Architectural registers in instructions are not logical registers. Also Fig. 15 does not show a register allocation

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table (RAT) but only illustrates that architectural registers in instructions can be mapped to rename registers. Moreover, Fig. 15 does not show, expressly or inherently, initializing the RAT. Thus, Fig. 15 of Levy does not teach or suggest this limitation recited in claim 23.

Second, the Examiner asserted that Levy's embodiment 1 discloses the limitation of dividing a freelist of registers in half if a processor associated with the freelist is in multi-thread mode because Levy's embodiment 1 discloses segregating rename register by thread. Applicants again respectfully disagree. The Examiner's characterization of Levy's embodiment 1 may be correct, but Levy's embodiment 1 does not disclose a freelist of registers nor does it disclose dividing the freelist in half. Such specific limitations cannot be inferred from Levy's embodiment 1. Levy's embodiment 1 physically partitions architectural and renaming registers into different sets, each set for a thread; and a register in one set for one thread cannot be used by another register even though that register is free (e.g., in a free list) (see col. 9, line 67 through col. 10, line 4 of Levy). Thus, Levy's embodiment 1 does not have a freelist of registers and does not always divide registers in half because if there are 3 threads, all registers will be partitioned in 3 sets. Therefore, Levy's embodiment 1 does not teach or suggest this limitation recited in claim 23.

Because Levy at least does not teach or suggest the limitation of initializing a register allocation table to map a first group of logical registers to a second group of physical registers or the limitation of dividing a freelist of registers in half if a processor associated with the freelist is in multi-thread mode, Levy does not anticipate independent claim 23. Accordingly, Levy does not anticipated all of the claims that

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depend from claim 23 (i.e., claims 24-30). Therefore, Applicants respectfully request that the 35 U.S.C. § 102(b) rejections of claims 23-30 based on Levy be withdrawn.

Claim Rejections – 35 U.S.C. § 103

Claims 1-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Levy in view of Leibholz (U.S. Patent No. 6, 954,846) (hereinafter Leibholz).

The Examiner admitted, "Levy fails to disclose that the physical registers are to be divided equally among a plurality of threads when operating in MT mode," but the Examiner that Leibholz discloses physical registers being divided equally among a plurality of threads when operating in MT mode by citing col. 1, lines 56-67 and col. 4, lines 19-20 of Leibholz. Applicants respectfully disagree. Col. 1, lines 56-67 are quoted below (emphases added):

> The present invention addresses some of the limitations found with conventional microprocessors by providing a microprocessor that is capable of executing in either a multi-thread mode or a single thread mode. In the multi-thread mode, *each active thread may have an associated register file* which the thread may access. In the single thread mode, *a single thread is active and the thread has access to all of the available register files.* In one embodiment of the present invention, *two threads may simultaneously execute and there are two register files. In the single thread mode, the single active thread may have access to both of the register files.*

Applicants cannot find from the cited portion of Leibholz (as quoted above) anything, expressly or inherently, that physical registers in a physical register file are to be divided equally among a plurality of threads when operating in MT mode, as recited in claim 1. Instead, the quoted portion of Leibholz discloses that each thread has its own register file when there are multi-thread and when operating in a single thread mode, the single thread may access to all of the register files. There is no dividing of any registers in a

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register file here in the cited portion of Leibholz; nor has dividing equally even been mentioned, or required expressly or inherently here in the cited portion of Leibholz. Since the Examiner also cited col. 4, lines 19-20 of Leibholz in rejecting the limitation at issue in claim 1, this portion along with its context are quoted below (emphasis added:

> In contrast, in single thread mode, the logical register name 25 (See FIG. 2B) is mapped to two physical registers 27 and 29 in the respective register files 20A and 20B. The registers 20A and 20B hold *identical contents*.

Again Applicants cannot find the above-quoted portion of Leibholz has anything related to dividing physical registers in a register file equally when operating in MT mode, as recited in claim 1. Rather this portion of Leibholz teaches away of dividing registers but rather using two registers to hold the same contents when operating in a single thread mode.

For the foregoing reasons, Leibholz does not teach or suggest the limitation of dividing physical registers in a register file equally when operating in MT mode, as recited in claim 1. Hence, the combination of Levy and Leibholz does not render this limitation obvious under 35 U.S.C. § 103(a). Claim 1 is thus patentable over Levy in view of Leibholz.

The same limitation of dividing physical registers in a register file equally when operating in MT mode is also recited in independent claims 8 and 16. For the foregoing reasons, the combination of Levy and Leibholz does not teach or suggest this limitation. Thus, independent claims 8 and 16 are patentable over Levy in view of Leibholz.

Because independent claims 1, 8, and 16 are now patentable over Levy in view of Leibholz, all of the claims that depend therefrom (i.e., claims 2-7, 10-15, and 17-22)

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are also patentable over Levy in view of Leibholz. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejections of claims 1-22 be withdrawn.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in condition for allowance, and their passage to issuance is respectfully solicited. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

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